REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-26 and 34-36 were pending and rejected. In this response, claims 1, 7, 18, and 34 have been amended to particularly point out and distinctly claim, in full, clear, concise, and exact terms, the subject matter which Applicants regard as their invention. Claims 2 and 35 have been canceled. New dependent claims 65-66 have been added. No new matter has been added.

Rejections under 35 U.S.C. § 103

Claims 1-2, 7-10, 18-21, and 34-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, US 6,868,504 (hereinafter "Lin") in view of Lo et al., US Publication 2003/0102894 (hereinafter "Lo").

Claim 1, as amended, recites:

> 1. A programmable delay cell comprising:
> a capacitor coupled to a low supply rail;
> a conductor coupled to an output of said programmable delay cell; and
> two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor, **wherein an impedance of each of said pass gates is to be controlled by a respective control signal**. (Emphasis added)

Applicants submit that Lin and Lo fail to disclose at least "wherein an impedance of each of said pass gates is to be controlled by a respective control signal" as required in claim 1. Referring to Lin, Lin discloses a delay line for use in phase locked loop and delay locked loop circuits (Figure 3a). Lin describes that load can be adjusted through operation of switches 47-54 (column 3, line 67 to column 4, line 17). There is no mention of pass gates and control signals in Lin's disclosure. Lo is relied on to disclose the limitation. However, the control signal of both pass gates is a same control signal such that the pass gates function as one buffer as intended (Lo, Figure 14). Therefore, Lo also fails to disclose "wherein an impedance of each of said pass gates is to be controlled by a respective control signal". Lin and Lo, even if combined, would still fail to teach all the elements of claim 1.

Furthermore, Lo discloses using pass gates as a buffer, but fails to teach controlling impedance of each of the pass gates. Thus, one skilled in the art would not look into Lo for controlling impedance of each of pass gates. Therefore, it is not obvious to combine Lin and Lo.

At least for the foregoing reasons, Applicants submit that claim 1 is not obvious over Lin and Lo. Applicants respectfully request that the rejection for claim 1 under 103(a) be withdrawn.

Claims 7, 18, and 34, as amended, require "wherein an impedance of each of said pass gates is to be controlled by a respective control signal". Applicants would like to submit that Lin and Lo fail to teach at least this limitation. Detailed remarks with respect to claim 1 are incorporated herein by reference.

At least for the foregoing reasons, Applicants believe that claims 7, 18, and 34 are not obvious over Lin and Lo. Claims 8-10 and 19-21, depending from claims 7 and 18 respectively, are also allowable for at least the same reason. Applicants respectfully request that the rejections for the claims be withdrawn.

Claim 3 and 36 are rejected under 35 U.S.C. 103(a) as being obvious over Lin in view of Lo and Sharp, US 4,584,492 (hereinafter "Sharp"). Claim 3 and 36, depending from claims 1 and 34 respectively, are not obvious over Lin and Lo. As set forth above, Lin and Lo do not disclose "wherein an impedance of each of said pass gates is to be controlled by a respective control signal". Sharp does not cure the deficiency of Lin and Lo.

Moreover, both claims 3 and 36 require a variable impedance transistor. Sharp is relied upon to disclose the limitation. Sharp describes a circuit comprising transistors (transistors 14-16, 21-23) including transistor 23. Transistor 23 is configured to be a reference potential to input inverter 24. Sharp states that "transistor 23 [a]ffects the input to the inverter 24 in the same manner as transistor 16 [a]ffects the input to inverter 17" and "the current through transistor 16 [a]ffects the buffered reference potential on line 19 …." (Line 19 is the input to inverter 17) (Sharp, col. 3, lines 28-43). Therefore, transistor 23 is not "a variable impedance transistor" as required in claims 3 and 36.

Additionally, all the transistors are n-channel enhancement mode transistors (Sharp, col. 3, lines 49-51). Sharp shows a circuit comprising many components to compensate for temperature and power supply changes. All the transistors in Sharp are of specific sizes. For example, transistors 21, 20, and 23 must be identical to transistors 14, 15, and 16 (Sharp, col. 4, lines 21-25). Sharp requires all transistors to be preselected and matched so that the compensation circuit is operable. In short, Sharp does not disclose "a variable impedance transistor" as required in claims 3 and 36. At least for the foregoing reasons, Applicants believe that claims 3 and 36 are not obvious over Lin, Lo, and Sharp. Applicants respectfully request that the rejections for the claims be withdrawn.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being obvious over Lin in view of Sharp. Claim 4, as presented, recites:

> 4. A programmable delay cell comprising:
> a conductor coupled to an output of said programmable delay cell;
> a switch transistor coupled to the conductor; and

> **a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal**. (Emphasis added)

Applicants would like to submit that Lin and Sharp fail to disclose at least "a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal" as required in claim 4. The Office Action admits that Lin does not disclose "a variable impedance transistor". Sharp is relied on to cure the deficiency.

As explained above with respect to claim 3, Sharp discloses transistor 23 that is configured to be a reference potential to input inverter 24. Sharp states that "transistor 23 [a]ffects the input to the inverter 24 in the same manner as transistor 16 [a]ffects the input to inverter 17" and "the current through transistor 16 [a]ffects the buffered reference potential on line 19 ...." (Line 19 is the input to inverter 17) (Sharp, col. 3, lines 28-43). Therefore, transistor 23 is not "a variable impedance transistor" as required in claim 4.

Claims 12-16 and 22-26 are rejected under 35 U.S.C. 103(a) as being obvious over Lin in view of Sharp. Both claims 12 and 22 require "a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal". Applicants would like to submit that both Lin and Sharp fail to disclose at least this limitation. Detailed remarks with respect to claim 3 are incorporated herein by reference.

At least for the foregoing reasons, Applicants believe that claim 4, 12, 22 are not obvious over Lin and Sharp. Claims 5-6, 13-16, and 23-26 depending from claims 4, 12, and 22 are also allowable for at least the same reason. Applicants respectfully request that the rejections for the claims be withdrawn.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Lo, Ahmad, Indian Application No. 633/DEL/2003 (hereinafter "Ahmad"), and Nakahata, U.S. Patent No. 4,528,634 (hereinafter "Nakahata"). Applicants respectfully submit that Ahmad is a foreign application and therefore is not a proper prior art under 102(e) (MPEP, 2136.03 Critical Reference Date - 2100 Patentability).

Claim 11 depends from claim 7 which is not obvious over Lin and Lo as explained above. Ahmad and Nakahata fail to cure the deficiency of Lin and Lo with respect to claim 7.

Furthermore, claim 11 requires "one or two registers coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer." The Office Action alleges that Ahmad in view of Nakahata discloses the limitation. Applicants respectfully disagree. Ahmad shows a pull-up predriver, a pull-down predriver, and configuration bits (Ahmad, Figure 2). There is no association between configuration bits and driving impedance values of output pin (DATAOUT) in Ahmad. Therefore, Ahmad does not teach "a first value that determines the source driving impedance" and "a second value that determines the sink driving impedance of said output buffer". Nakahata also is silent with respect to disclosing "a first value that determines the source driving impedance" and "a second value that determines the sink driving impedance of said output buffer".

At least for the foregoing reasons, Applicants believe that claim 11 is not obvious over Lin, Lo, Ahmad, and Nakahata. Applicants respectfully request that the rejection for the claim be withdrawn.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Sharp, Ahmad, and Nahakata. As indicated above with respect to claim 11, Ahmad is not a proper prior art under 102(e).

Claim 17 depends from claim 12 which is allowable over Lin and Sharp. Ahmad and Nakahata fail to cure the deficiency of Lin and Sharp with respect to claim 12. Additionally, claim 17 requires "one or two registers coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer". As discussed, Ahmad and Nahakata fail to teach the limitation. Detailed remarks with respect to claim 11 are incorporated herein by reference.

At least for the foregoing reasons, Applicants believe that claim 17 is not obvious over Lin, Sharp, Ahmad, and Nakahata. Applicants respectfully request that the rejection for the claim be withdrawn.

New Claims

Applicants have presented two new dependent claims. Claim 65 depends from claim 1 and claim 66 depends from claim 4. In view of the foregoing reasons, independent claims 1 and 4 are allowable and therefore the dependent claims 65-66 are also allowable over the cited references.

Claim 65 requires "wherein the two or more pass gates comprise at least four pass gates". The cited references fail to teach the limitations as set forth in the claims above. In particular, Lo discloses replacing each transistor with only a pass gate to perform the intended function (as indicated in the Office Action in the comparison of Figure 7 and Figure 14 in Lo).

Claim 66 requires "wherein a first terminal of the variable impedance transistor is coupled to a high supply rail and a second terminal of the variable impedance transistor is coupled to only a source terminal of the switch transistor" (emphasis added). Referring to Sharp, transistor 23 is connected to two nodes including a terminal of transistor 20 and the input to inverter 24 (Sharp, Figure 1). Therefore, Sharp fails to disclose at least the limitation required in claim 66.

Therefore, at least for the foregoing reasons, Applicants submit that claims 65-66 are allowable over the cited references. Applicants respectfully request the allowance for claims 65-66.

CONCLUSION

In view of the foregoing, Applicants respectfully submit the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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